University of Bahrain
College of Information Technology
Department of Computer Engineering

ITCE 202: Digital Logic
Test II

Time: 1:00 hour

Date: December 14, 2004

Question	Marks	Scor
1	20	
2	20	
3	20	
4	20	
5	20	
Total	100	

ID. No.	Name:	Sec.:

Show all your work.

Q1 (20 points)

A combinational Logic Circuit accepts two 4-bit binary numbers $A = A_3\ A_2\ A$ $B = B_3\ B_2\ B_1\ B_0$ and generates a single output Z such that:

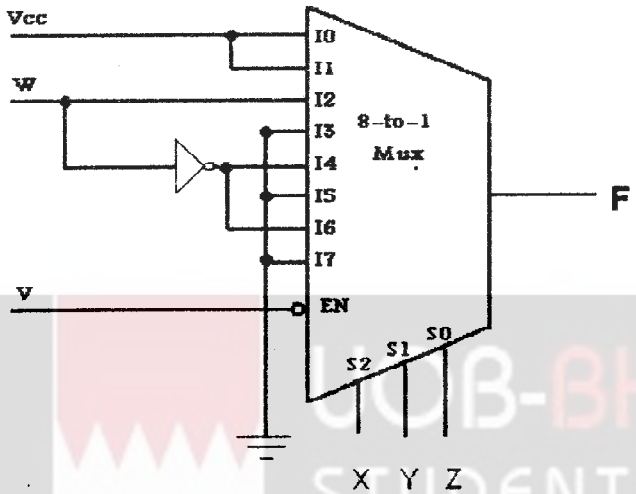
$Z = 1$ if $A + B + 7 \geq 12$ else $Z = 0$

Use any necessary ICs and logic gates to implement the combinational circuit.

Q2(20 points)

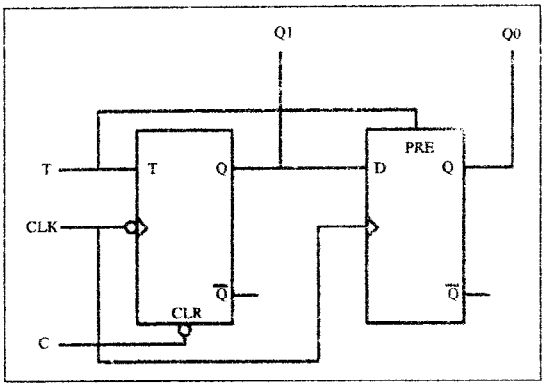
Use 3-to-8 decoder(s) with enable to implement a code converter combinatio that takes as its inputs an Execss-3 code digit and outputs its equivalent BCD d

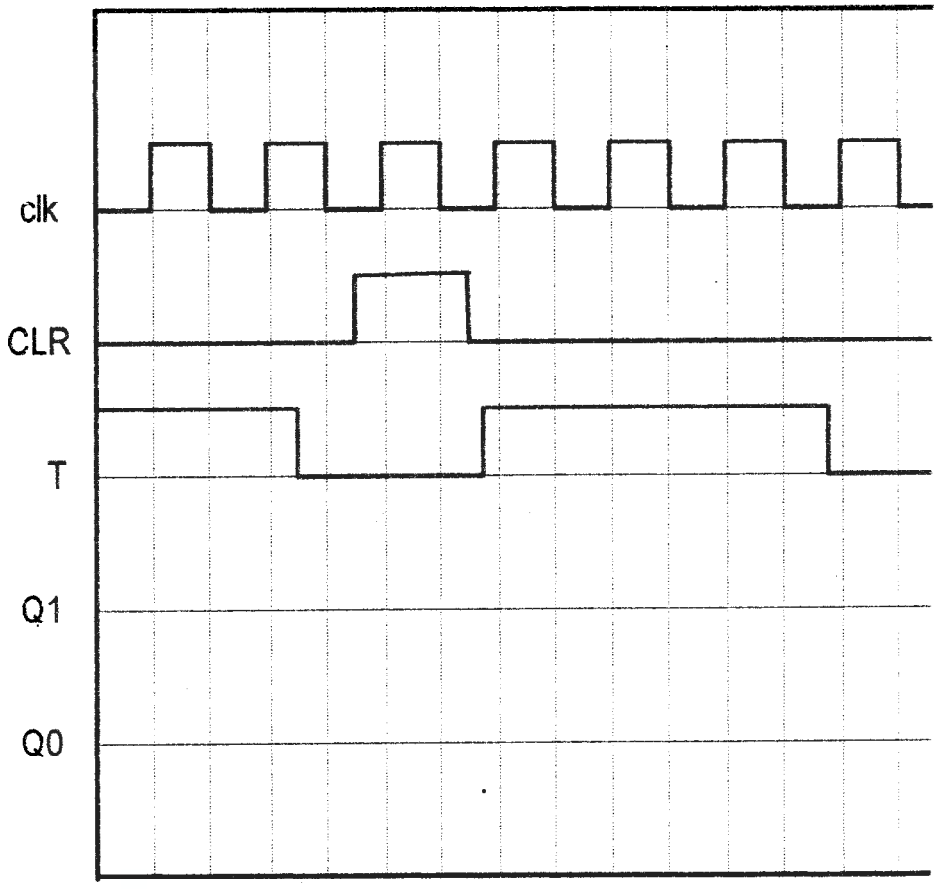
Q3(20 points)
Express F in a S-O-P form (Do not simplify)



Q4(20 points)

Complete the following timing diagram for the circuit shown below.





Q5(20 points)

A gated Latch has two inputs G, and L behaves as follows: If G = 0 th not change its state. If G=1, the next state of the latch is equal to its inpu

(a) Derive the characteristic equation of the G-L latch.

(b) Show how a J-K latch can be converted to a G-L latch.